

### FEATURES

- 44 V supply maximum rating**
- $V_{SS}$  to  $V_{DD}$  analog signal range**
- Single-/dual-supply specifications**
- Wide supply ranges (10.8 V to 16.5 V)**
- Extended plastic temperature range**  
( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )
- Low power dissipation (28 mW maximum)**
- Low leakage (20 pA typical)**
- Available in 16-lead DIP/SOIC\_N and 20-lead  
PLCC/LCC packages**
- Superior alternative to:**  
**DG508A, HI-508**  
**DG509A, HI-509**

### FUNCTIONAL BLOCK DIAGRAMS

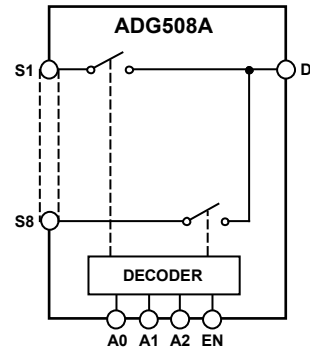


Figure 1. ADG508A

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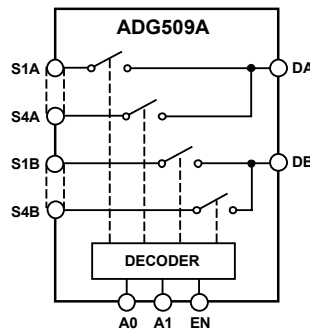


Figure 2. ADG509A

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### GENERAL DESCRIPTION

The ADG508A and ADG509A are CMOS monolithic analog multiplexers with eight channels and dual four channels, respectively. The ADG508A switches one of eight inputs to a common output, depending on the state of three binary addresses and an enable input. The ADG509A switches one of four differential inputs to a common differential output, depending on the state of two binary addresses and an enable input. Both devices have TTL and 5 V CMOS logic-compatible digital inputs.

The ADG508A and ADG509A are designed on an enhanced LC<sup>2</sup>MOS process that gives an increased signal capability of  $V_{SS}$  to  $V_{DD}$  and enables operation over a wide range of supply voltages. The devices can comfortably operate anywhere in the 10.8 V to 16.5 V single- or dual-supply range. These multiplexers also feature high switching speeds and low  $R_{ON}$ .

### PRODUCT HIGHLIGHTS

1. Single-/Dual-Supply Specifications with a Wide Tolerance. The devices are specified in the 10.8 V to 16.5 V range for both single and dual supplies.
2. Extended Signal Range. The enhanced LC<sup>2</sup>MOS processing results in a high breakdown and an increased analog signal range of  $V_{SS}$  to  $V_{DD}$ .
3. Break-Before-Make Switching. Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
4. Low Leakage. Leakage currents in the range of 20 pA make these multiplexers suitable for high precision circuits.

#### Rev. C

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## REVISION HISTORY

### 3/07—Rev. B to Rev. C

Updated Format .....	Universal
Changes to Table 3 .....	6
Inserted Table 4 .....	7
Inserted Table 6 .....	8
Changes to Figure 24.....	12
Updated Outline Dimensions .....	13
Changes to Ordering Guide .....	15

## SPECIFICATIONS

## DUAL SUPPLY

$V_{DD} = 10.8 \text{ V to } 16.5 \text{ V}$ ,  $V_{SS} = -10.8 \text{ V to } -16.5 \text{ V}$ , unless otherwise noted.

Table 1.

Parameter	ADG508A ADG509A K Version		ADG508A ADG509A B Version		ADG508A ADG509A T Version		Unit	Comments
	+25°C	-40°C to +85°C	+25°C	-40°C to +85°C	+25°C	-55°C to +125°C		
ANALOG SWITCH								
Analog Signal Range	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	V min	
	$V_{DD}$	$V_{DD}$	$V_{DD}$	$V_{DD}$	$V_{DD}$	$V_{DD}$	V max	
$R_{ON}$	280		280		280		$\Omega$ typ	$-10 \text{ V} \leq V_S \leq +10 \text{ V}$ , $I_{DS} = 1 \text{ mA}$ ; see Figure 14
	450	600	450	600	450	600	$\Omega$ max	
	300	400	300	400			$\Omega$ max	$V_{DD} = 15 \text{ V} (\pm 10\%)$ , $V_{SS} = -15 \text{ V} (\pm 10\%)$
					300	400	$\Omega$ max	$V_{DD} = 15 \text{ V} (\pm 5\%)$ , $V_{SS} = -15 \text{ V} (\pm 5\%)$
$R_{ON}$ Drift	0.6		0.6		0.6		%/°C typ	$V_S = 0$ , $I_{DS} = 1 \text{ mA}$
$R_{ON}$ Match	5		5		5		% typ	$-10 \text{ V} \leq V_S \leq +10 \text{ V}$ , $I_{DS} = 1 \text{ mA}$
$I_S$ (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	$V_1 = \pm 10 \text{ V}$ , $V_2 = \mp 10 \text{ V}$ ; see Figure 15
	1	50	1	50	1	50	nA max	
$I_D$ (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	$V_1 = \pm 10 \text{ V}$ , $V_2 = \mp 10 \text{ V}$ ; see Figure 16
ADG508A	1	100	1	100	1	100	nA max	
ADG509A	1	50	1	50	1	50	nA max	
$I_D$ (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	$V_1 = V_2 = \pm 10 \text{ V}$ ; see Figure 17
ADG508A	1	100	1	100	1	100	nA max	
ADG509A	1	50	1	50	1	50	nA max	
$I_{DIFF}$ , Differential Off Output Leakage (ADG509A only)		25		25		25	nA max	$V_1 = \pm 10 \text{ V}$ , $V_2 = \mp 10 \text{ V}$ ; see Figure 18
DIGITAL CONTROL								
$V_{INH}$ , Input High Voltage		2.4		2.4		2.4	V min	
$V_{INL}$ , Input Low Voltage		0.8		0.8		0.8	V max	
$I_{INL}$ or $I_{INH}$		1		1		1	$\mu\text{A}$ max	$V_{IN} = 0$ to $V_{DD}$
$C_{IN}$ Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS								
$t_{TRANSITION}^1$	200		200		200		ns typ	$V_1 = \pm 10 \text{ V}$ , $V_2 = \mp 10 \text{ V}$ ; see Figure 19
	300	400	300	400	300	400	ns max	
$t_{OPEN}^1$	50		50		50		ns typ	See Figure 20
	25	10	25	10	25	10	ns min	
$t_{ON} (EN)^1$	200		200		200		ns typ	See Figure 21
	300	400	300	400	300	400	ns max	
$t_{OFF} (EN)^1$	200		200		200		ns typ	See Figure 21
	300	400	300	400	300	400	ns max	
OFF Isolation	68		68		68		dB typ	$V_{EN} = 0.8 \text{ V}$ , $R_L = 1 \text{ k}\Omega$ , $C_L = 15 \text{ pF}$ , $V_S = 7 \text{ V rms}$ , $f = 100 \text{ kHz}$
	50		50		50		dB min	
$C_S$ (OFF)	5		5		5		pF typ	$V_{EN} = 0.8 \text{ V}$
$C_D$ (OFF)								
ADG508A	22		22		22		pF typ	$V_{EN} = 0.8 \text{ V}$
ADG509A	11		11		11		pF typ	
$Q_{INU}$ , Charge Injection	4		4		4		pC typ	$R_S = 0 \Omega$ , $V_S = 0$ ; see Figure 22

# ADG508A/ADG509A

Parameter	ADG508A ADG509A K Version		ADG508A ADG509A B Version		ADG508A ADG509A T Version		Unit	Comments
	+25°C	-40°C to +85°C	+25°C	-40°C to +85°C	+25°C	-55°C to +125°C		
POWER SUPPLY								
I <sub>DD</sub>	0.6		0.6		0.6		mA typ	V <sub>IN</sub> = V <sub>INL</sub> or V <sub>INH</sub>
		1.5		1.5		1.5	mA max	
I <sub>SS</sub>	20		20		20		μA typ	V <sub>IN</sub> = V <sub>INL</sub> or V <sub>INH</sub>
		0.2		0.2		0.2	mA max	
Power Dissipation	10		10		10		mW typ	
		28		28		28	mW max	

<sup>1</sup> Sample tested at 25°C to ensure compliance.

## SINGLE SUPPLY

$V_{DD} = 10.8\text{ V to }16.5\text{ V}$ ,  $V_{SS} = \text{GND} = 0\text{ V}$ , unless otherwise noted.

**Table 2.**

Parameter	ADG508A ADG509A K Version		ADG508A ADG509A B Version		ADG508A ADG509A T Version		Unit	Comments
	+25°C	-40°C to +85°C	+25°C	-40°C to +85°C	+25°C	-55°C to +125°C		
<b>ANALOG SWITCH</b>								
Analog Signal Range	GND	GND	GND	GND	GND	GND	V min	
	$V_{DD}$	$V_{DD}$	$V_{DD}$	$V_{DD}$	$V_{DD}$	$V_{DD}$	V max	
$R_{ON}$	500		500		500		$\Omega$ typ	$\text{GND} \leq V_S \leq +10\text{ V}$ , $I_{DS} = 0.5\text{ mA}$ ; see Figure 14
	700	1000	700	1000	700	1000	$\Omega$ max	
$R_{ON}$ Drift	0.6		0.6		0.6		%/°C typ	$V_S = 0$ , $I_{DS} = 0.5\text{ mA}$
$R_{ON}$ Match	5		5		5		% typ	$\text{GND} \leq V_S \leq +10\text{ V}$ , $I_{DS} = 0.5\text{ mA}$
$I_S$ (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	$V_1 = +10\text{ V/GND}$ , $V_2 = \text{GND}/+10\text{ V}$ ; see Figure 15
	1	50	1	50	1	50	nA max	
$I_D$ (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	$V_1 = +10\text{ V/GND}$ , $V_2 = \text{GND}/+10\text{ V}$
ADG508A	1	100	1	100	1	100	nA max	See Figure 16
ADG509A	1	50	1	50	1	50	nA max	
$I_D$ (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	$V_1 = V_2 = +10\text{ V/GND}$ ; see Figure 17
ADG508A	1	100	1	100	1	100	nA max	
ADG509A	1	50	1	50	1	50	nA max	
$I_{DIFF}$ , Differential Off Output Leakage (ADG509A only)		25		25		25	nA max	$V_1 = +10\text{ V/GND}$ , $V_2 = \text{GND}/+10\text{ V}$ ; see Figure 18
<b>DIGITAL CONTROL</b>								
$V_{INH}$ , Input High Voltage		2.4		2.4		2.4	V min	
$V_{INL}$ , Input Low Voltage		0.8		0.8		0.8	V max	
$I_{INL}$ or $I_{INH}$		1		1		1	$\mu\text{A}$ max	$V_{IN} = 0$ to $V_{DD}$
$C_{IN}$ Digital Input Capacitance	8		8		8		pF max	
<b>DYNAMIC CHARACTERISTICS</b>								
$t_{TRANSITION}^1$	300		300		300		ns typ	$V_1 = +10\text{ V/GND}$ , $V_2 = \text{GND}/+10\text{ V}$ ; see Figure 19
	450	600	450	600	450	600	ns max	
$t_{OPEN}^1$	50		50		50		ns typ	See Figure 20
	25	10	25	10	25	10	ns min	
$t_{ON}$ (EN) <sup>1</sup>	250		250		250		ns typ	See Figure 21
	450	600	450	600	450	600	ns max	
$t_{OFF}$ (EN) <sup>1</sup>	250		250		250		ns typ	See Figure 21
	450	600	450	600	450	600	ns max	
OFF Isolation	68		68		68		dB typ	$V_{EN} = 0.8\text{ V}$ , $R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , $V_S = 3.5\text{ V rms}$ , $f = 100\text{ kHz}$
	50		50		50		dB min	
$C_S$ (OFF)	5		5		5		pF typ	$V_{EN} = 0.8\text{ V}$
$C_D$ (OFF)								
ADG508A	22		22		22		pF typ	$V_{EN} = 0.8\text{ V}$
ADG509A	11		11		11		pF typ	
$Q_{INJ}$ , Charge Injection	4		4		4		pC typ	$R_S = 0\ \Omega$ , $V_S = 0\text{ V}$ ; see Figure 22
<b>POWER SUPPLY</b>								
$I_{DD}$	0.6		0.6		0.6		mA typ	$V_{IN} = V_{INL}$ or $V_{INH}$
		1.5		1.5		1.5	mA max	
Power Dissipation	10		10		10		mW typ	
		25		25		25	mW max	

<sup>1</sup> Sample tested at 25°C to ensure compliance.

# ADG508A/ADG509A

## ABSOLUTE MAXIMUM RATINGS

T<sub>A</sub> = 25°C, unless otherwise noted.


Table 3.

Parameter	Ratings
V <sub>DD</sub> to V <sub>SS</sub>	44 V
V <sub>DD</sub> to GND	32 V
V <sub>SS</sub> to GND	-32 V
Analog Inputs <sup>1</sup> Voltage at S, D	V <sub>SS</sub> - 2 V to V <sub>DD</sub> + 2 V or 20 mA, whichever occurs first
Continuous Current, S or D	20 mA
Pulsed Current S or D 1 ms Duration, 10% Duty Cycle	40 mA
Digital Inputs <sup>1</sup> Voltage at A, EN	V <sub>SS</sub> - 4 V to V <sub>DD</sub> + 4 V or 20 mA, whichever occurs first
Power Dissipation (Any Package) Up to 75°C Derates Above 75°C by	470 mW 6 mW/°C
Operating Temperature Commercial (K Version)	-40°C to +85°C
Industrial (B Version)	-40°C to +85°C
Extended (T Version)	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

<sup>1</sup>Overvoltage at A, EN, S, or D is clamped by diodes. Current should be limited to the maximum rating shown in Table 3.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION

	<b>ESD (electrostatic discharge) sensitive device.</b> Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
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## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

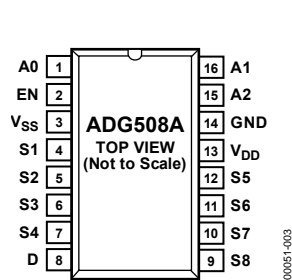


Figure 3. ADG508A DIP, SOIC\_N

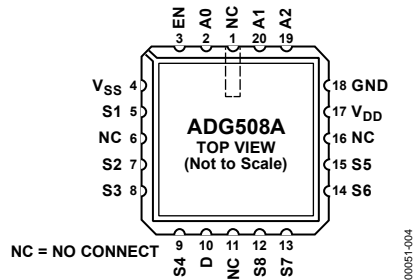


Figure 4. ADG508A LCC

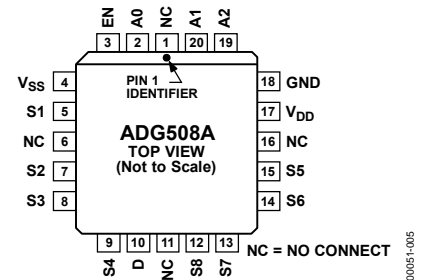


Figure 5. ADG508A PLCC

Table 4. ADG508A Pin Function Description

Pin Number		Mnemonic	Description
DIP/SOIC_N	PLCC/LCC		
1	2	A0	Logic Control Input.
2	3	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
3	4	V <sub>SS</sub>	Most Negative Power Supply Potential in Dual Supplies. In single-supply applications, it can be connected to ground.
4	5	S1	Source Terminal 1. Can be an input or an output.
5	7	S2	Source Terminal 2. Can be an input or an output.
6	8	S3	Source Terminal 3. Can be an input or an output.
7	9	S4	Source Terminal 4. Can be an input or an output.
8	10	D	Drain Terminal. Can be an input or an output.
9	12	S8	Source Terminal 8. Can be an input or an output.
10	13	S7	Source Terminal 8. Can be an input or an output.
11	14	S6	Source Terminal 7. Can be an input or an output.
12	15	S5	Source Terminal 6. Can be an input or an output.
13	17	V <sub>DD</sub>	Source Terminal 5. Can be an input or an output.
14	18	GND	Ground (0V) Reference.
15	19	A2	Logic Control Input.
16	20	A1	Logic Control Input.
N/A	1	NC	No Connect.
N/A	6	NC	No Connect.
N/A	11	NC	No Connect.
N/A	16	NC	No Connect.

Table 5. ADG508A Truth Table

A2	A1	A0	EN	ON SWITCH
x	x	x	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

# ADG508A/ADG509A

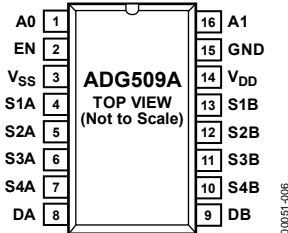


Figure 6. ADG509A DIP, SOIC\_N

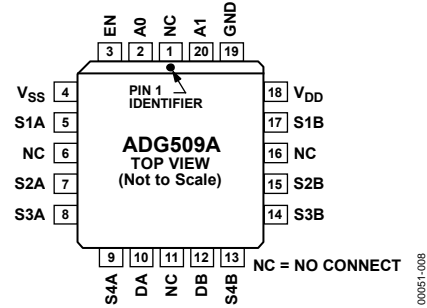


Figure 7. ADG509A PLCC

Table 6. ADG509A Pin Function Description

Pin Number		Mnemonic	Description
DIP/SOIC	PLCC/LCC		
1	2	A0	Logic Control Input.
2	3	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
3	4	V <sub>SS</sub>	Most Negative Power Supply Potential in Dual Supplies. In single-supply applications, it can be connected to ground.
4	5	S1A	Source Terminal 1A. Can be an input or an output.
5	7	S2A	Source Terminal 2A. Can be an input or an output.
6	8	S3A	Source Terminal 3A. Can be an input or an output.
7	9	S4A	Source Terminal 4A. Can be an input or an output.
8	10	DA	Drain Terminal A. Can be an input or an output.
9	12	DB	Drain Terminal B. Can be an input or an output.
10	13	S4B	Source Terminal 4B. Can be an input or an output.
11	14	S3B	Source Terminal 3B. Can be an input or an output.
12	15	S2B	Source Terminal 2B. Can be an input or an output.
13	17	S1B	Source Terminal 1B. Can be an input or an output.
14	18	V <sub>DD</sub>	Most Positive Power Supply Potential.
15	19	GND	Ground (0 V) Reference.
16	20	A1	Logic Control Input.
N/A	1	NC	No Connect.
N/A	6	NC	No Connect.
N/A	11	NC	No Connect.
N/A	16	NC	No Connect.

Table 7. ADG509A Truth Table

A1	A0	EN	ON SWITCH PAIR
x	x	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

x = don't care



## TYPICAL PERFORMANCE CHARACTERISTICS

The multiplexers are guaranteed functional with reduced single or dual supplies down to 4.5 V.

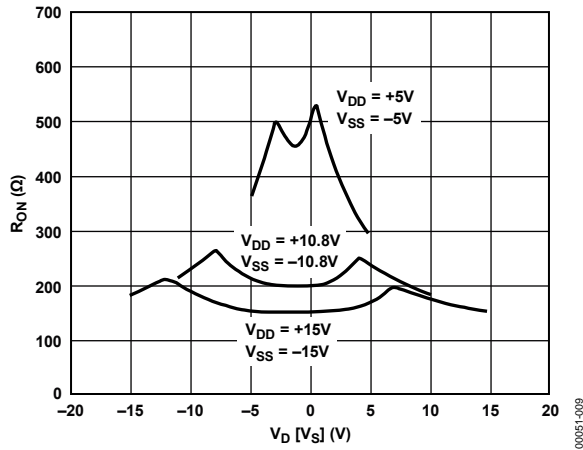


Figure 8.  $R_{ON}$  as a Function of  $V_D$  ( $V_s$ ): Dual-Supply Voltage,  $T_A = 25^\circ C$

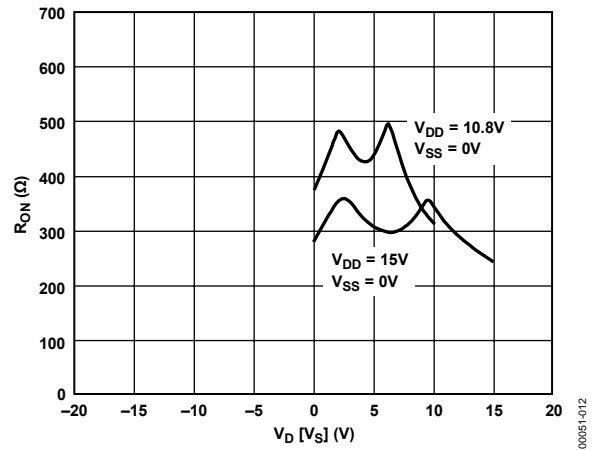


Figure 11.  $R_{ON}$  as a Function of  $V_D$  ( $V_s$ ) Single-Supply Voltage,  $T_A = 25^\circ C$

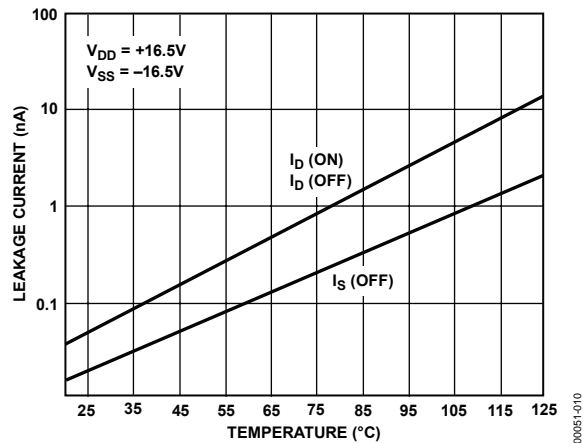


Figure 9. Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)

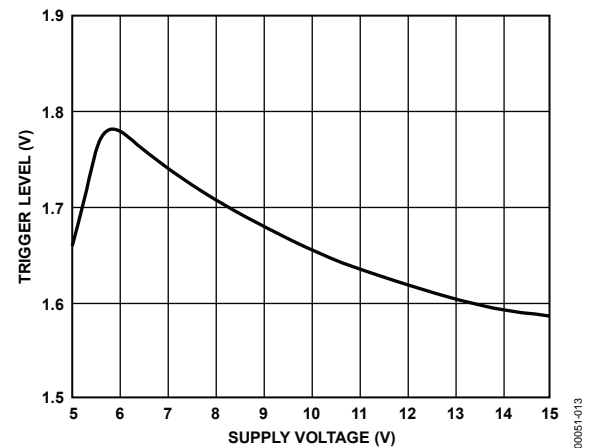


Figure 12. Trigger Levels vs. Power Supply Voltage, Dual or Single Supply,  $T_A = 25^\circ C$

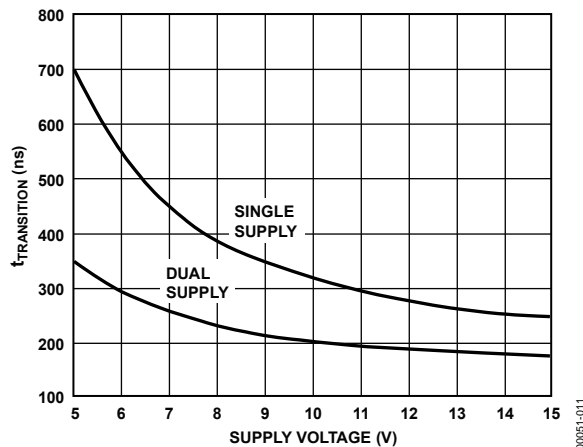


Figure 10.  $t_{TRANSITION}$  vs. Supply Voltage: Dual and Single Supplies,  $T_A = 25^\circ C$  (Note: For  $V_{DD}$  and  $V_{SS1} < 10 V$ ;  $V1 = V_{DD}/V_{SS}$ ,  $V2 = V_{SS}/V_{DD}$ . (see Figure 19))

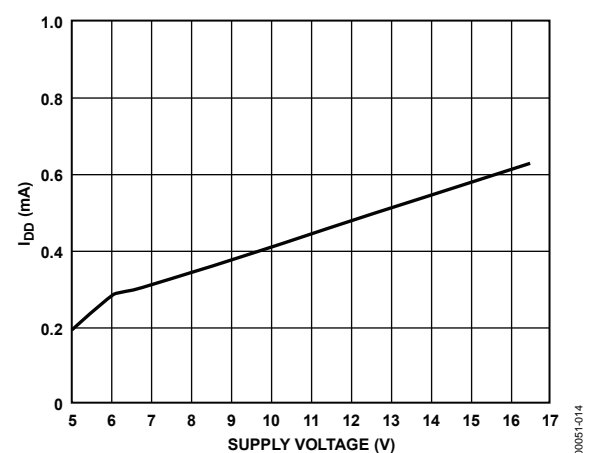


Figure 13.  $I_{DD}$  vs. Supply Voltage: Dual or Single Supply,  $T_A = 25^\circ C$

# ADG508A/ADG509A

## TEST CIRCUITS

Note: All digital input signal rise and fall times measured from 10% to 90% of 3 V.  $t_R = t_F = 20$  ns.

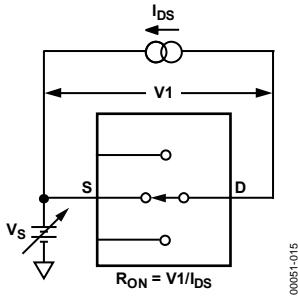


Figure 14.  $R_{ON}$

00051-015

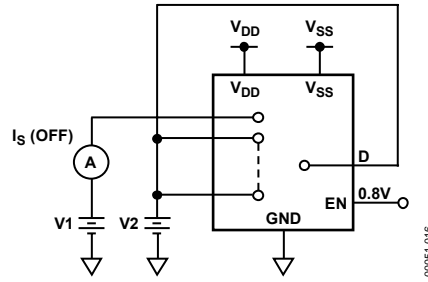


Figure 15.  $I_S$  (OFF)

00051-016

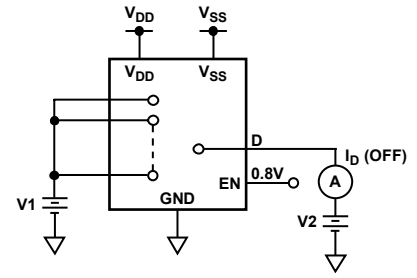


Figure 16.  $I_D$  (OFF)

00051-017

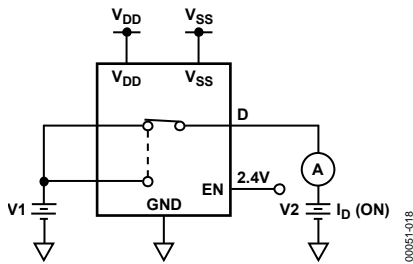


Figure 17.  $I_D$  (ON)

00051-018

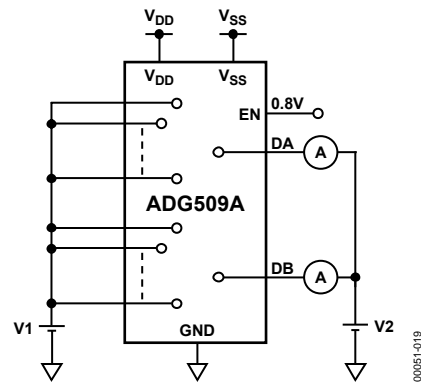


Figure 18.  $I_{DIFF} = I_{DB}$  (OFF)

00051-019

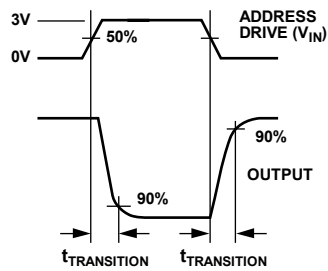
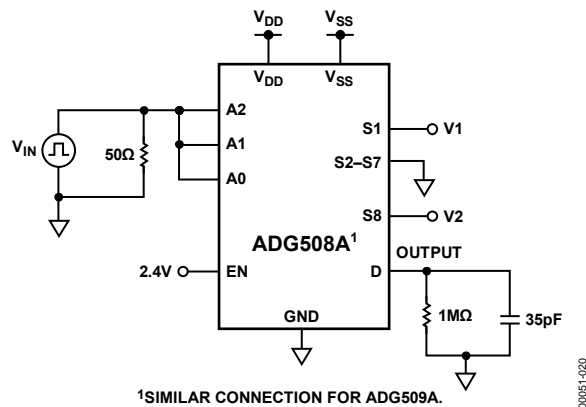


Figure 19. Switching Time of Multiplexer,  $t_{TRANSITION}$



<sup>1</sup>SIMILAR CONNECTION FOR ADG509A.

00051-020

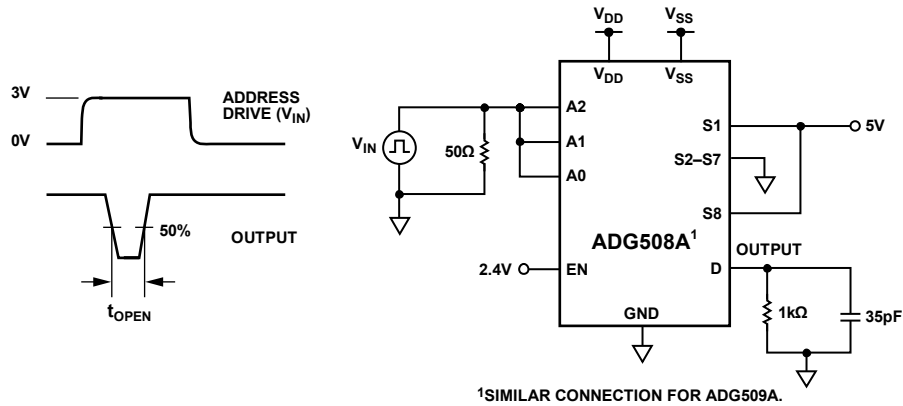


Figure 20. Break-Before-Make Delay,  $t_{OPEN}$

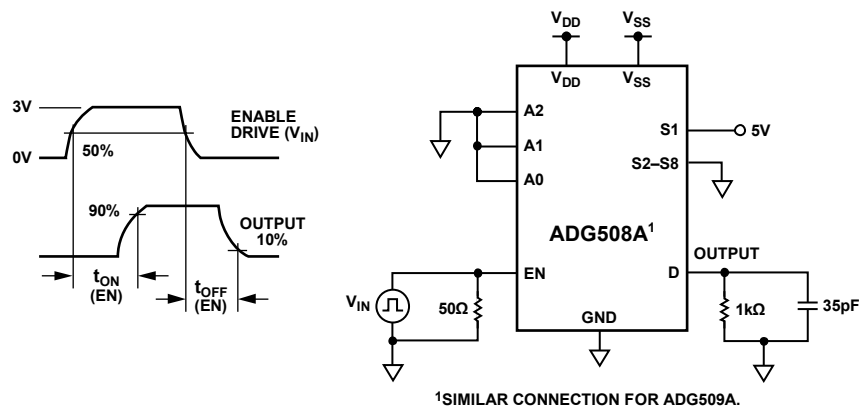


Figure 21. Enable Delay,  $t_{ON}(EN)$ ,  $t_{OFF}(EN)$

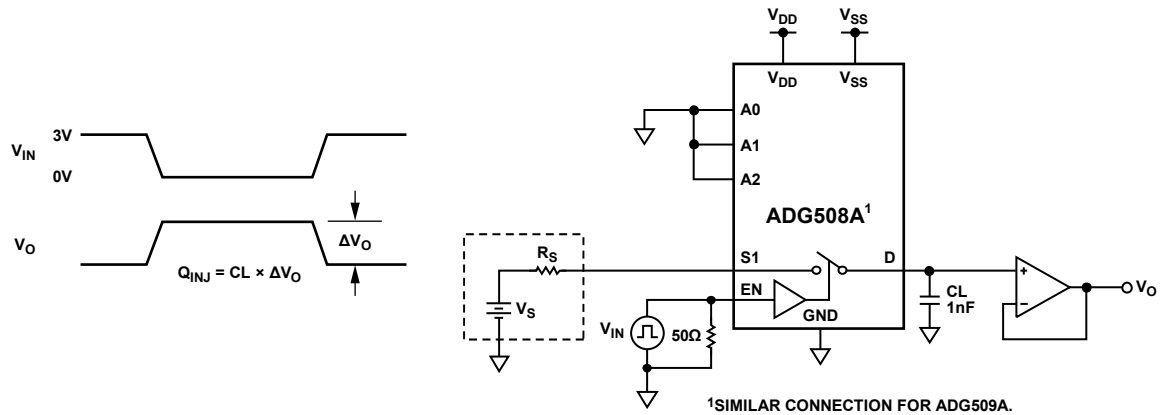


Figure 22. Charge Injection

# ADG508A/ADG509A

## SINGLE-SUPPLY OCTAL DAC APPLICATION

The following circuit shows the ADG508A connected as a demultiplexer to provide eight separate, digitally programmable voltages (0 V to 10 V) from the AD7245A. The AD7245A is a complete 12-bit, voltage output DAC with output amplifier and Zener voltage reference on a monolithic CMOS chip.

The entire system operates from a single 15 V power supply. The ADG508A is ideally suited for the application because it has both low charge injection and  $I_S$  (OFF) leakage current.

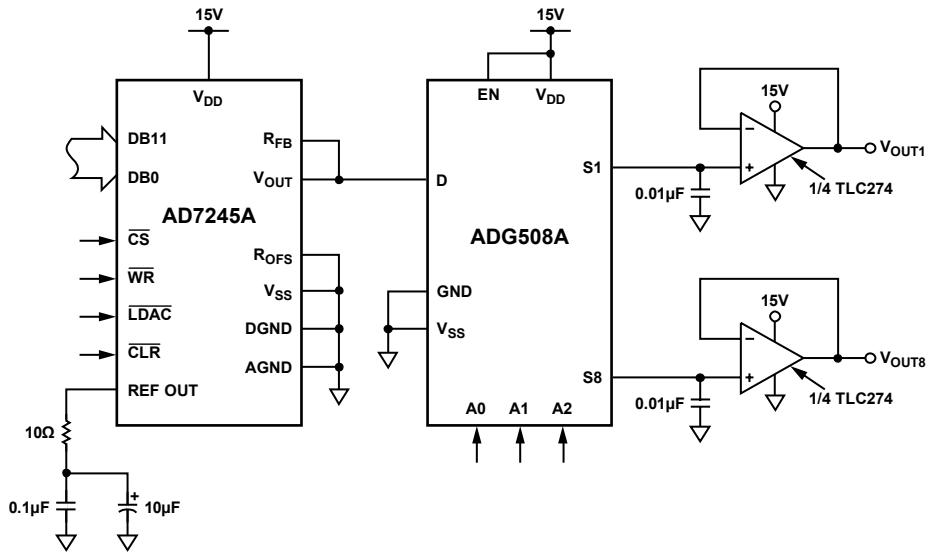
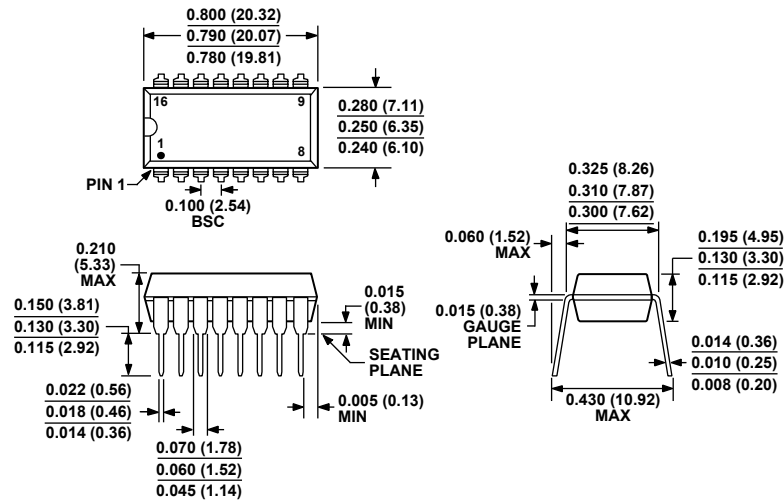


Figure 23. ADG508A in a Single-Supply Octal DAC Circuit

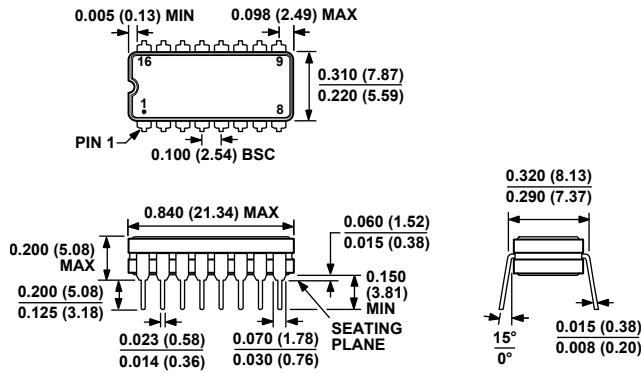
00051-024

OUTLINE DIMENSIONS



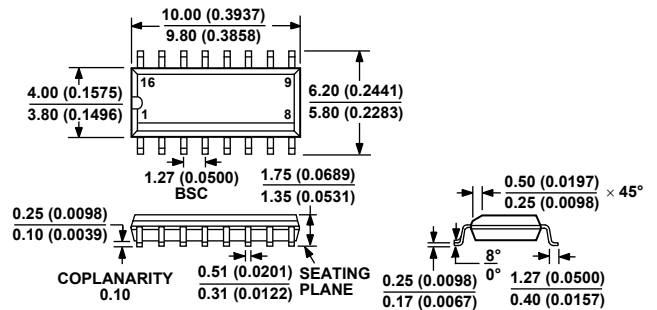
COMPLIANT TO JEDEC STANDARDS MS-001-AB  
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 24. 16-Lead Plastic Dual In-Line Package [PDIP] Narrow Body (N-16)  
 Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

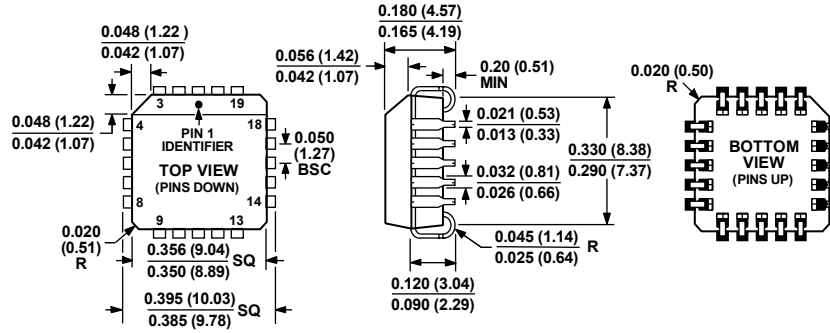
Figure 25. 16-Lead Ceramic Dual In-Line Package [CERDIP] (Q-16)  
 Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AC  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 26. 16-Lead Standard Small Outline Package [SOIC\_N] Narrow Body (R-16)  
 Dimensions shown in inches and (millimeters)

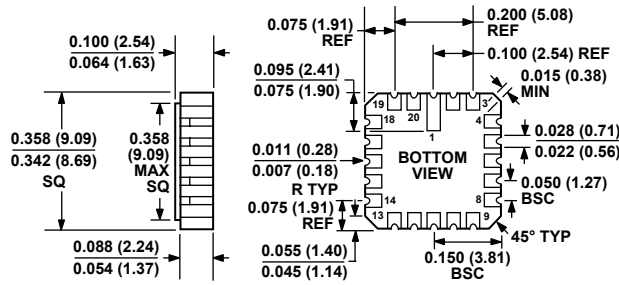
# ADG508A/ADG509A



COMPLIANT TO JEDEC STANDARDS MO-047-AA  
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 27. 20-Lead Plastic Leaded Chip Carrier [PLCC]  
 (P-20)

Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 28. 20-Terminal Ceramic Leadless Chip Carrier [LCC]  
 (E-20)

Dimensions shown in inches and (millimeters)

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG508AKN	-40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG508AKNZ <sup>1</sup>	-40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG508AKR	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG508AKR-REEL	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG508AKR-REEL7	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG508AKRZ <sup>1</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG508AKRZ-REEL <sup>1</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG508AKRZ-REEL7 <sup>1</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG508AKP	-40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20
ADG508AKP-REEL	-40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20
ADG508AKPZ <sup>1</sup>	-40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20
ADG508AKPZ-REEL <sup>1</sup>	-40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20
ADG508ABQ	-40°C to +85°C	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16
ADG508ATQ	-55°C to +125°C	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16
ADG508ATE	-55°C to +125°C	20-Terminal Ceramic Leadless Chip Carrier [LCC]	E-20
ADG508ABCHIPS		DIE	
ADG508ATCHIPS		DIE	
ADG509AKN	-40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG509AKNZ <sup>1</sup>	-40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG509AKR	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG509AKR-REEL	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG509AKR-REEL7	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG509AKRZ-REEL <sup>1</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG509AKRZ-REEL7 <sup>1</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG509AKP	-40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20
ADG509AKP-REEL	-40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20
ADG509AKPZ <sup>1</sup>	-40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20
ADG509AKPZ-REEL <sup>1</sup>	-40°C to +85°C	20-Lead Plastic Leaded Chip Carrier [PLCC]	P-20
ADG509ABQ	-40°C to +85°C	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16
ADG509ATQ	-55°C to +125°C	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16
ADG509ATQ/883B	-55°C to +125°C	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q16
ADG509ABCHIPS		DIE	
ADG509ATCHIPS		DIE	

<sup>1</sup> Z = Pb-free part.

**NOTES**